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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,680	10/13/2000	Ville Eerola	PM 274422/2990978US	7630

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EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 04/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/689,680	EEROLA ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to amendment filed on 1/17/06 in which claims 1-22 are pending. The applicant's amendments have been fully considered but they are moot based on the new ground of rejection.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 9-15, 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Carlson U.S. Patent No 4,833,479.

As per claim 1, Carlson discloses a device for generating a t least one code phase, comprising: a delay circuit is the same as the claimed (shift register) (see fig.1 element 22 or 24 and col.2, lines 58-67) comprising N outputs and input to which a in-phase or quadrature sample is the same as the claimed (code sequence) (see fig.1 element I or Q and col.1, lines 65-67 and col.2, lines 1-5) to be phased is applied, N being an integer greater than two; a correlator is considered as the claimed (at least one logic branch) (see fig.1 element 25 or 36 and col.2, lines 63-67) controlled by at least a EEPROM is the same as the claimed (one combination control signal) (see fig.1 element 40 and col.3, lines 2-5)), on the basis of which the logic branch adds is considered as the claimed (combines) (see col.3, lines 1-65 and col.9, lines 15-35) the code phase from I outputs of the shift register, I being an integer between 2 and N

wherein said EEPROM (combination control signal) is usable to set one or more weighting coefficients (see col.2, lines 5-10 and col.3, lines 4, lines 60-65 and col.5, lines 15-20 and col.8, lines 5-30).

As per claim 2, the device of Carlson does include a two input multiplier is the same as the claimed (I two-input selectors) (see fig.1 elements 26-29 and col.2, lines 63-65 and col.3, lines 1-10, 48-55), to the first input of each of which is connected one input of the shift register and to the second input is connected one EEPROM (combination control signal) (see fig.1 element 40) and adders is considered as the claimed (I-input combiner) (see fig.1 element 32-33), to whose outputs are connected the outputs of said I selectors and from whose output said code phase is obtained.

As per claim 3, the device of Carlson does include a first logic branch (see fig.1 element 25) comprising M1 a two input multiplier is the same as the claimed (I two-input selectors) (see fig.1 elements 26-29) to which the outputs of M1 registers of the shift register and M1 EEPROM (combination control signals) are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and M1-input adders is considered as the claimed (M1-input combiner) (see fig.1 element 32), to whose inputs are connected the outputs of said M1 selectors and from whose output the first code phase is obtained (see fig.7, 11-13) ; a second logic branch (see fig.1 element 30) comprising M2 two input multiplier is the same as the claimed (I two-input selectors) (see fig.1 elements 26-29) to which the outputs of M2 registers of the shift register and M2 EEPROM (combination control) signals are connected in such a way that to the inputs of each selector is connected one

output of the shift register and one combination control signal, and an adder is considered as the claimed (M2-input combiner) (see fig.1 element 33) to whose inputs are connected the outputs of said M2 selectors and from whose output the second code phase is obtained.

As per claim 9, the device Carlson teaches the logic branches changed by software (see col.5, lines 29-31).

As per claim 10, the device of Carlson teaches multipliers and/or AND gates (see fig.1 elements 26-29).

As per claim 11, the device of Carlson does include are adders and/or OR gates (see fig.1 elements 32-33).

As per claim 12, the device of Carlson teaches weighting coefficients. (see col.5, lines 15-20 and col.8, lines 10-29).

As per claim 13, the device of Carlson discloses a correlator (see fig.1 elements 25 or 30 and col.2, lines 63-64) comprising: a in-phase or quadrature sample is the same as the claimed (generation means comprising a code generator for generating local code) (see fig.1 element I or Q and col.1, lines 65-67 and col.2, lines 1-5) and a delay circuit is the same as the claimed (shift register) (see fig.1 element 22 or 24 and col.2, lines 58-67), the (I or Q) (generation means generating at least one code phase from said local code); at least one correlator (see col.1, lines 43-45) for correlating a signal applied to the correlator structure with said at least on locally generated code phase, said generation means further comprising a multiply and add circuit is considered as the claimed (at least one logic branch) (see fig.1 element 25 or 36 and

col.2, lines 63-67) controlled by at least a EEPROM is the same as the claimed (one combination control signal) (see fig.1 element 40 and col.3, lines 2-5)), on the basis of which the logic branch adds is considered as the claimed (combines) (see col.3, lines 1-65 and col.9, lines 15-35) the code phase from I outputs of the shift register, I being an integer between 2 and N wherein said EEPROM (combination control signal) is usable to set one or more weighting coefficients (see col.2, lines 5-10 and col.3, lines 4, lines 60-65 and col.5, lines 15-20 and col.8, lines 5-30).

As per claim 14, the correlator of Carlson does include a two input multiplier is the same as the claimed (I two-input selectors) (see fig.1 elements 26-29 and col.2, lines 63-65 and col.3, lines 1-10, 48-55), to the first input of each of which is connected one input of the shift register and to the second input is connected one EEPROM (combination control signal) (see fig.1 element 40) and adders is considered as the claimed (I-input combiner) (see fig.1 element 32-33), to whose outputs are connected the outputs of said I selectors and from whose output said code phase is obtained.

As per claims 15 and 18, the correlator of Carlson teaches the logic branches changed by software (see col.5, lines 29-331).

As per claims 20-21, the device of Carlson teaches one or more weighting coefficients (see col.8, lines 5-30).

Claim Rejections - 35 USC ٤ 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Carlson U.S. Patent No 4,833,479 in view of Nakamura et al U.S. Patent NO 6,275,520

B.

1. As per claims 4-6, Carlson teaches all the features of the claimed invention except a third logic branch connected directly to the output of one register of the shift register and from which the third code phase is obtained.

Nakamura et al teaches a third branch (see figs.2, 9 element 16) connected directly to the output of one register of the shift registers (see fig.2 element 10) and from which the third code phase is obtained (see col.1, lines 36-45 and col.2, lines 60-65).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Nakamura into Carlson as to provide desired shift amounts and each pattern would be prestored in the storage location in the ROM as taught by Nakamura (see col.2, lines 63-65).

As per claims 7-8, Carlson teaches all the features of the claimed invention except a fourth logic branch connected directly to the output of one register of the shift register and from which the third code phase is obtained.

Nakamura et al teaches a fourth branch (see figs.2, 9 element 16) connected directly to the output of one register of the shift registers (see fig.2 element 10) and from which the third code phase is obtained (see col.1, lines 36-45 and col.2, lines 60-65).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Nakamura into Carlson as to provide desired shift amounts and each pattern would be prestored in the storage location in the ROM as taught by Nakamura (see col.2, lines 63-65).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 16-19 and 22 rejected under 35 U.S.C. 102(e) as being anticipated by Oishi et al U.S. Patent No 6,650,689 B1.

As per claim 16, Oishi et al discloses a spread spectrum receiver for receiving a spread spectrum signal the spread spectrum receiver comprising (see figs. 3,10) : generation means comprising a code generator for generating local code) (see fig.10 element 21) and a delay circuit is the same as the claimed (shift register) (see fig.10 element 22a or D1-Dm), the generation means generating at least one code phase from said local code); at least one correlator (see figs.3, 10 element 23 and abstract col.8, lines 27-29) for correlating a signal applied to the correlator structure with said at least on locally generated code phase, said generation means further comprising a multiply and add circuit is considered as the claimed (at least one logic branch) (see figs.3, 10

element 22) controlled by at least one combination control signal)(see figs.3, 10 element 22b) on the basis of which the logic branch adds is considered as the claimed (combines) (see figs. 3, 10 element 22c) the code phase from I outputs of the shift register, I being an integer between 2 and N wherein said EEPROM (combination control signal) is usable to set one or more weighting coefficients (see elements W1-Wm and col.10, lines 5-6).

As per claim 17, the device of Oishi et al does include a two input multiplier is the same as the claimed (I two-input selectors) (see figs. 3, 10 elements MP1 or MPm), to the first input of each of which is connected one input of the shift register and to the second input is connected to (combination control signal) (see fig.3, 10 element 22b) and adders is considered as the claimed (I-input combiner) (see fig.3, 10 element 22c), to whose outputs are connected the outputs of said I selectors and from whose output said code phase is obtained

As per claim 18, the correlator of Oishi et al inherently teaches means generation are changed by software.

As per claim 19 the device of the correlator of Oishi et al inherently teaches a phase spreading code replica.

As per claim 22, the device of the correlator of Oishi et teaches one or more weighting coefficients (see figs. 3, 10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272

3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571 272 2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2611

3/29/06

EMMANUEL BAYARD
PRIMARY EXAMINER